

#### Features

- Integrated analog input Class D audio amplifier driver in a small 16 pin package
- Floating inputs enable easy half bridge implementation
- Programmable bidirectional over-current protection with self-reset function
- Programmable preset deadtime for improved THD performances
- Start and stop click noise reduction
- High noise immunity
- $\pm 100\text{ V}$  ratings deliver up to 500 W in output power
- Operates up to 800 kHz
- RoHS compliant

#### Product Summary

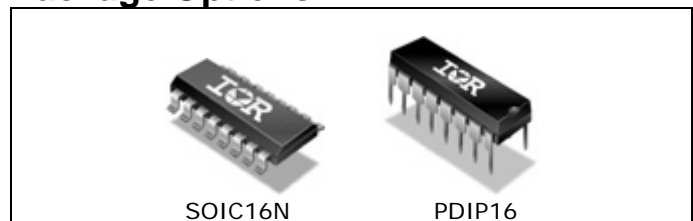
$V_{\text{OFFSET}}$ (max)		$\pm 100\text{ V}$
Gate driver	Io+	1.0 A
	Io-	1.2 A
Selectable Deadtime		25/40/65/105 ns
OC protection delay (max)		500 ns
DC offset		<20 mV
PWM frequency		~800 kHz
Error amplifier open loop gain		>60 dB
THD+N* (1kHz, 50W, 4 $\Omega$ )		0.01 %
Residual Noise* (AES-17 Filter)		200 $\mu\text{Vrms}$

\* measured with recommended circuit

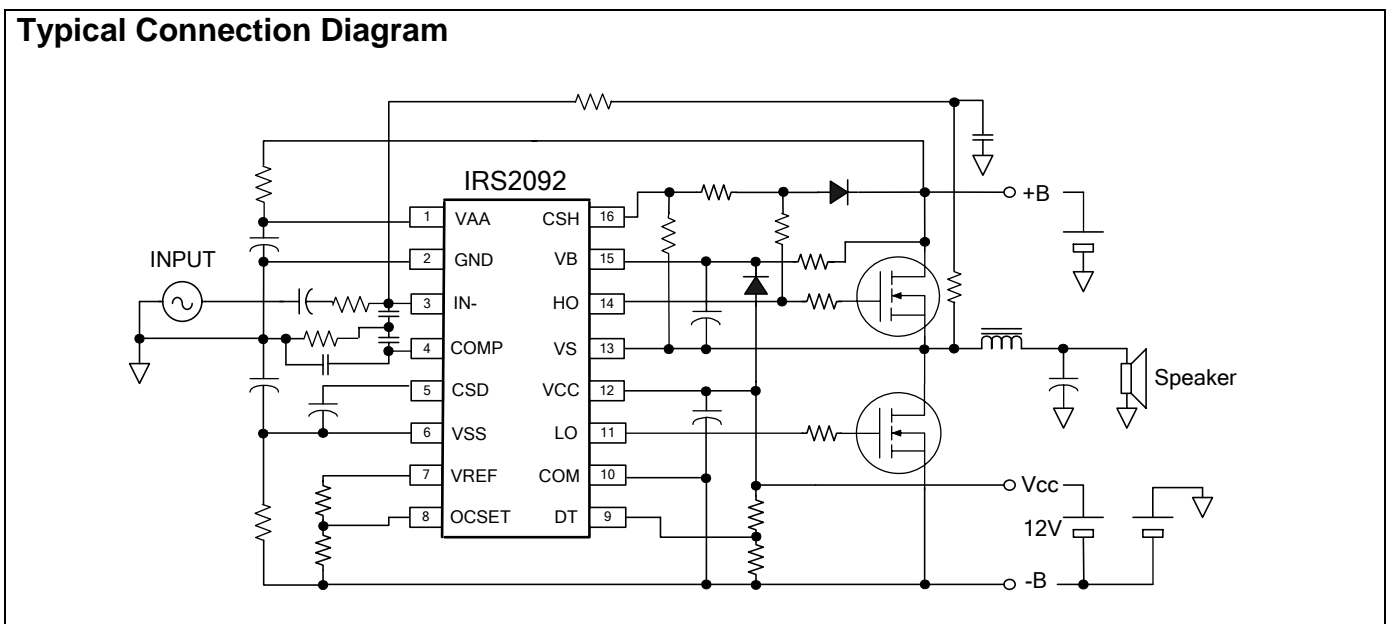
#### Typical Applications

- Home theater systems
- Mini component stereo systems
- Powered speaker systems
- General purpose audio power amplifiers

#### Package Options



#### Typical Connection Diagram



**Description**

The IRS2092 is a high voltage, high performance Class D audio amplifier driver with PWM modulator and protection. In conjunction with two external MOSFET and a few external components, a complete Class D audio amplifier with protection can be realized.

International Rectifier's proprietary noise isolation technology allows high current gate drive stage and high speed low noise error amplifier reside on a single small silicon die.

Open elements of PWM modulator section allow flexible PWM topology implementation.

**Absolute Maximum Ratings**

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min	Max	Units	
V <sub>B</sub>	High side floating supply voltage	-0.3	220	V	
V <sub>S</sub>	High side floating supply voltage (Note2)	V <sub>B</sub> -20	V <sub>B</sub> +0.3		
V <sub>HO</sub>	High side floating output voltage	V <sub>S</sub> -0.3	V <sub>B</sub> +0.3		
V <sub>CSH</sub>	CSH pin input voltage	V <sub>S</sub> -0.3	V <sub>B</sub> +0.3		
V <sub>CC</sub>	Low side fixed supply voltage (Note2)	-0.3	20		
V <sub>LO</sub>	Low side output voltage	-0.3	V <sub>CC</sub> +0.3		
V <sub>AA</sub>	Floating input positive supply voltage (Note2)	(See I <sub>AAZ</sub> )	210		
V <sub>SS</sub>	Floating input negative supply voltage (Note2)	-1 (See I <sub>SSZ</sub> )	GND +0.3		
V <sub>GND</sub>	Floating input supply ground voltage	V <sub>SS</sub> -0.3 (See I <sub>SSZ</sub> )	V <sub>AA</sub> +0.3 (See I <sub>AAZ</sub> )		
I <sub>IN-</sub>	Inverting input current (Note1)	---	±3	mA	
V <sub>CSD</sub>	SD pin input voltage	V <sub>SS</sub> -0.3	V <sub>AA</sub> +0.3	V	
V <sub>COMP</sub>	COMP pin input voltage	V <sub>SS</sub> -0.3	V <sub>AA</sub> +0.3		
V <sub>DT</sub>	DT pin input voltage	-0.3	V <sub>CC</sub> +0.3		
V <sub>OCSET</sub>	OCSET pin input voltage	-0.3	V <sub>CC</sub> +0.3		
I <sub>AAZ</sub>	Floating input positive supply zener clamp current (Note2)	---	20	mA	
I <sub>SSZ</sub>	Floating input negative supply zener clamp current (Note2)	---	20		
I <sub>CCZ</sub>	Low side supply zener clamp current (Note3)	---	10		
I <sub>BSZ</sub>	Floating supply zener clamp current (Note3)	---	10		
I <sub>OREF</sub>	Reference output current	---	5		
dV <sub>S</sub> /dt	Allowable V <sub>s</sub> voltage slew rate	---	50	V/ns	
dV <sub>SS</sub> /dt	Allowable V <sub>ss</sub> voltage slew rate (Note3)	---	50	V/ms	
Pd	Maximum power dissipation @ T <sub>A</sub> ≤ +25°C	SOIC16N	---	1.0	W
		DIP16	---	1.6	
Rth <sub>JA</sub>	Thermal resistance, Junction to ambient	SOIC16N	---	115	°C/W
		DIP16	---	75	
T <sub>J</sub>	Junction Temperature	---	150	°C	
T <sub>S</sub>	Storage Temperature	-55	150	°C	
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	---	300	°C	

Note1: IN- contains clamping diode to GND.

Note2: V<sub>DD</sub> – IN+, GND -V<sub>SS</sub>, V<sub>CC</sub>-COM and V<sub>B</sub>-V<sub>S</sub> contain internal shunt zener diodes. Please note that the voltage ratings of these can be limited by the clamping current.

Note3: For the rising and falling edges of step signal of 10 V. V<sub>SS</sub>=15 V to 200 V.

### Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions below. The  $V_S$  and COM offset ratings are tested with supplies biased at  $V_{AA}-V_{SS}=10$  V,  $V_{CC}=12$  V and  $V_B-V_S=12$  V. All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead.

Symbol	Definition	Min.	Max.	Units	
$V_B$	High side floating supply absolute voltage	$V_S + 10$	$V_S + 18$	V	
$V_S$	High side floating supply offset voltage	(Note 1)	200		
$I_{AAZ}$	Floating input positive supply zener clamp current	1	11	mA	
$I_{SSZ}$	Floating input negative supply zener clamp current	1	11		
$V_{SS}$	Floating input supply absolute voltage	0	200	V	
$V_{HO}$	High side floating output voltage	$V_S$	$V_B$		
$V_{CC}$	Low side fixed supply voltage	10	18		
$V_{LO}$	Low side output voltage	0	$V_{CC}$		
$V_{GND}$	GND pin input voltage	$V_{SS}$ (Note 3)	$V_{AA}$ (Note 3)		
$V_{IN-}$	Inverting input voltage	$V_{GND} - 0.5$	$V_{GND} + 0.5$		
$V_{CSD}$	CSD pin input voltage	$V_{SS}$	$V_{AA}$		
$V_{COMP}$	COMP pin input voltage	$V_{SS}$	$V_{AA}$		
$C_{COMP}$	COMP pin phase compensation capacitor to GND	1	-		nF
$V_{DT}$	DT pin input voltage	0	$V_{CC}$		V
$I_{OREF}$	Reference output current to COM (Note 2)	0.3	0.8	mA	
$V_{OCSET}$	OCSET pin input voltage	0.5	5		
$V_{CSH}$	CSH pin input voltage	$V_S$	$V_B$	V	
dVss/dt	Allowable Vss voltage slew rate upon power-up (Note4)	-	50	V/ms	
$I_{PW}$	Input pulse width	10 (Note 5)	-	ns	
$f_{SW}$	Switching Frequency	-	800	kHz	
$T_A$	Ambient Temperature	-40	125	°C	

Note 1: Logic operational for  $V_S$  equal to  $-5$  V to  $+200$  V. Logic state held for  $V_S$  equal to  $-5$  V to  $-V_{BS}$ .

Note 2: Nominal voltage for  $V_{REF}$  is 5.1 V.  $I_{OREF}$  of 0.3 – 0.8 mA dictates total external resistor value on  $V_{REF}$  to be 6.3 k $\Omega$  to 16.7 k $\Omega$ .

Note 3: GND input voltage is limited by  $I_{AAZ}$  and  $I_{SSZ}$ .

Note 4:  $V_{SS}$  ramps up from 0 V to 200 V.

Note 5: Output logic status may not respond correctly if input pulse width is smaller than the minimum pulse width.

## Electrical Characteristics

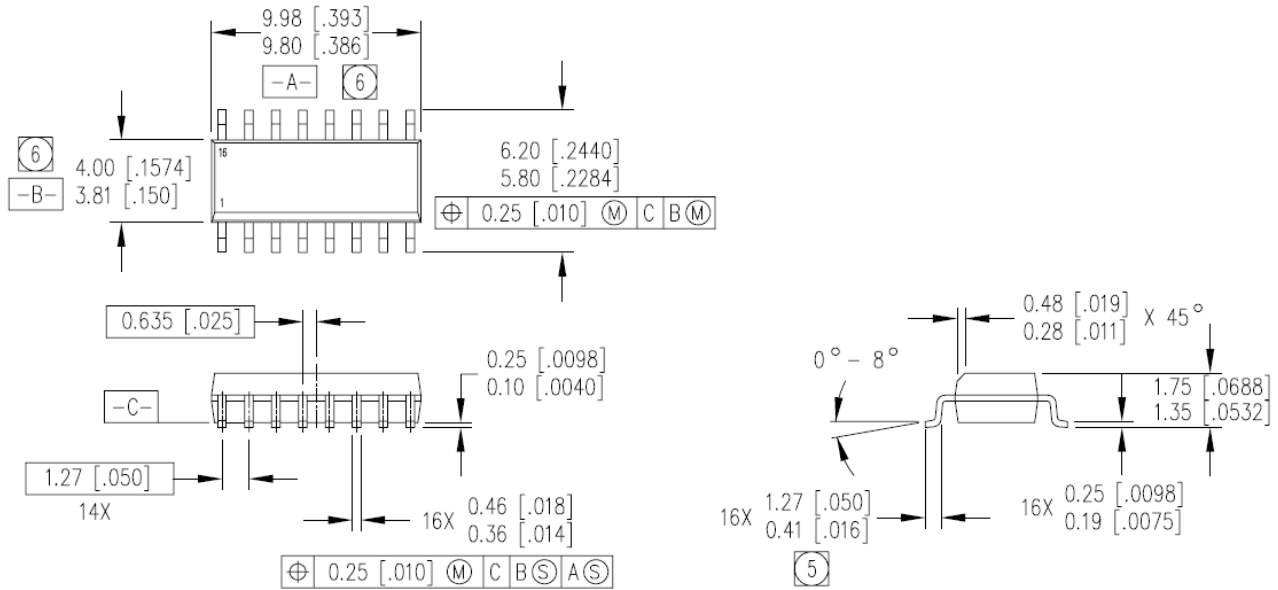
$V_{CC}, V_{BS} = 12\text{ V}$ ,  $V_{SS} = V_S = \text{COM} = 0\text{ V}$ ,  $V_{AA} = 10\text{ V}$ ,  $C_L = 1\text{ nF}$  and  $T_A = 25\text{ }^\circ\text{C}$  unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
<b>Low Side Supply</b>						
$UV_{CC+}$	Vcc supply UVLO positive threshold	8.4	8.9	9.4	V	
$UV_{CC-}$	Vcc supply UVLO negative threshold	8.2	8.7	9.2		
$UV_{CCHYS}$	$UV_{CC}$ hysteresis	-	0.2	-		
$I_{QCC}$	Low side quiescent current	-	-	3	mA	$V_{DT} = V_{CC}$
$V_{CLAMPL}$	Low side zener diode clamp voltage	19.6	20.4	21.6	V	$I_{CC} = 5\text{ mA}$
<b>High Side Floating Supply</b>						
$UV_{BS+}$	High side well UVLO positive threshold	8.0	8.5	9.0	V	
$UV_{BS-}$	High side well UVLO negative threshold	7.8	8.3	8.8		
$UV_{BSHYS}$	$UV_{BS}$ hysteresis	-	0.2	-		
$I_{QBS}$	High side quiescent current	-	-	1	mA	
$I_{LKH}$	High to Low side leakage current	-	-	50	$\mu\text{A}$	$V_B = V_S = 200\text{ V}$
$V_{CLAMPH}$	High side zener diode clamp voltage	19.6	20.4	21.6	V	$I_{BS} = 5\text{ mA}$
<b>Floating Input Supply</b>						
$UV_{AA+}$	$V_{AA+}$ , $V_{AA-}$ floating supply UVLO positive threshold from $V_{SS}$	8.2	8.7	9.2	V	$V_{SS} = 0\text{ V}$ , GND pin floating
$UV_{AA-}$	$V_{AA+}$ , $V_{AA-}$ floating supply UVLO negative threshold from $V_{SS}$	7.7	8.2	8.7		$V_{SS} = 0\text{ V}$ , GND pin floating
$UV_{AAHYS}$	$UV_{AA}$ hysteresis	-	0.5	-		$V_{SS} = 0\text{ V}$ , GND pin floating
$I_{QAA0}$	Floating Input positive quiescent supply current	-	0.5	2	mA	$V_{AA} = 10\text{ V}$ , $V_{SS} = 0\text{ V}$ , $V_{CSD} = V_{SS}$
$I_{QAA1}$	Floating Input positive quiescent supply current	-	8	11		$V_{AA} = 10\text{ V}$ , $V_{SS} = 0\text{ V}$ , $V_{CSD} = V_{AA}$
$I_{QAA2}$	Floating Input positive quiescent supply current	-	8	11		$V_{AA} = 10\text{ V}$ , $V_{SS} = 0\text{ V}$ , $V_{CSD} = \text{GND}$
$I_{LKM}$	Floating input side to Low side leakage current	-	-	50	$\mu\text{A}$	$V_{AA} = V_{SS} = V_{GND} = 100\text{ V}$
$V_{CLAMPM+}$	$V_{AA}$ floating supply zener diode clamp voltage, positive, with respect to GND	6.0	7.0	8.0	V	$I_{AA} = 5\text{ mA}$ , $I_{SS} = 5\text{ mA}$ , $V_{GND} = 0\text{ V}$ , $V_{CSD} = V_{SS}$
$V_{CLAMPM-}$	$V_{SS}$ floating supply zener diode clamp voltage, negative, with respect to GND	-8.0	-7.0	-6.0		$I_{AA} = 5\text{ mA}$ , $I_{SS} = 5\text{ mA}$ , $V_{GND} = 0\text{ V}$ , $V_{CSD} = V_{SS}$
<b>Audio Input (<math>V_{GND} = 0</math>, <math>V_{AA} = 5\text{ V}</math>, <math>V_{SS} = -5\text{ V}</math>)</b>						
$V_{OS}$	Input offset voltage	-15	0	15	mV	
$I_{BIN}$	Input bias current	-	-	40	nA	
BW	Small signal bandwidth	-	9	-	MHz	$C_{COMP} = 2\text{ nF}$ , $R_f = 3.3\text{ k}\Omega$
$V_{COMP}$	OTA Output voltage	$V_{AA} - 1$	-	$V_{SS} + 1$	V	
$g_m$	OTA transconductance	-	100	-	mS	$V_{IN} = 10\text{ mV}$
$G_V$	OTA gain	60	-	-	dB	
$V_{Nrms}$	OTA input noise voltage	-	250	-	mVrms	BW=20 kHz, Resolution BW=22 Hz Fig.5
SR	Slew rate	-	$\pm 5$	-	V/ $\mu\text{s}$	$C_{COMP} = 1\text{ nF}$
CMRR	Common-mode rejection ratio	-	60	-	dB	
PSRR	Supply voltage rejection ratio	-	65	-		
<b>PWM comparator</b>						
$V_{thPWM}$	PWM comparator threshold in COMP	-	$(V_{AA} - V_{SS})/2$	-	V	
$f_{OTA}$	COMP pin start-up local oscillation	0.7	1.0	1.5	MHz	$V_{CSD} = \text{GND}$

frequency					
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Protection						
V <sub>REF</sub>	Reference output voltage	4.8	5.1	5.4	V	I <sub>OREF</sub> = 0.5 mA
V <sub>thOCL</sub>	Low side OC threshold in Vs	1.1	1.2	1.3		OCSET=1.2 V, Fig.6
V <sub>thOCH</sub>	High side OC threshold in V <sub>CSH</sub>	1.1+ Vs	1.2+ Vs	1.3+ Vs		Vs=200 V,
V <sub>th1</sub>	CSD pin shutdown release threshold	0.62xV <sub>AA</sub>	0.70xV <sub>AA</sub>	0.78xV <sub>AA</sub>		
V <sub>th2</sub>	CSD pin self reset threshold	0.26xV <sub>AA</sub>	0.30xV <sub>AA</sub>	0.34xV <sub>AA</sub>		
I <sub>CSD+</sub>	CSD pin discharge current	70	100	130	μA	V <sub>CSD</sub> = V <sub>SS</sub> +5 V
I <sub>CSD-</sub>	CSD pin charge current	70	100	130		V <sub>CSD</sub> = V <sub>SS</sub> +5 V
t <sub>SD</sub>	Shutdown propagation delay from V <sub>CSD</sub> > V <sub>SS</sub> + V <sub>thOCH</sub> to Shutdown	-	-	250	ns	
t <sub>OCH</sub>	Propagation delay time from V <sub>CSH</sub> > V <sub>thOCH</sub> to Shutdown	-	-	500		Fig.3
t <sub>OCL</sub>	Propagation delay time from Vs > V <sub>thOCL</sub> to Shutdown	-	-	500		Fig.4
Gate Driver						
I <sub>o+</sub>	Output high short circuit current (Source)	-	1.0	-	A	V <sub>o</sub> =0 V, PW≤10 μs
I <sub>o-</sub>	Output low short circuit current (Sink)	-	1.2	-	A	V <sub>o</sub> =12 V, PW≤10 μs
V <sub>OL</sub>	Low level output voltage LO – COM, HO - VS	-	-	0.1	V	I <sub>o</sub> =0 A
V <sub>OH</sub>	High level output voltage VCC – LO, VB - HO	-	-	1.4		
t <sub>on</sub>	High and low side turn-on propagation delay	-	360	-	ns	V <sub>DT</sub> = V <sub>CC</sub>
t <sub>off</sub>	High and low side turn-off propagation delay	-	335	-		V <sub>DT</sub> = V <sub>CC</sub>
t <sub>r</sub>	Turn-on rise time	-	20	50		
t <sub>f</sub>	Turn-off fall time	-	15	35		
DT1	Deadtime: LO turn-off to HO turn-on (DT <sub>LO-HO</sub> ) & HO turn-off to LO turn-on (DT <sub>HO-LO</sub> )	15	25	35		V <sub>DT</sub> >V <sub>DT1</sub> ,
DT2	Deadtime: LO turn-off to HO turn-on (DT <sub>LO-HO</sub> ) & HO turn-off to LO turn-on (DT <sub>HO-LO</sub> )	25	40	55		V <sub>DT1</sub> >V <sub>DT</sub> > V <sub>DT2</sub> ,
DT3	Deadtime: LO turn-off to HO turn-on (DT <sub>LO-HO</sub> ) & HO turn-off to LO turn-on (DT <sub>HO-LO</sub> )	50	65	85		V <sub>DT2</sub> >V <sub>DT</sub> > V <sub>DT3</sub> ,
DT4	Deadtime: LO turn-off to HO turn-on (DT <sub>LO-HO</sub> ) & HO turn-off to LO turn-on (DT <sub>HO-LO</sub> ) V <sub>DT</sub> = V <sub>DT4</sub>	85	105	135		V <sub>DT3</sub> >V <sub>DT</sub> > V <sub>DT4</sub> ,
V <sub>DT1</sub>	DT mode select threshold 2	0.51xV <sub>CC</sub>	0.57xV <sub>CC</sub>	0.63xV <sub>CC</sub>	V	
V <sub>DT2</sub>	DT mode select threshold 3	0.32xV <sub>CC</sub>	0.36xV <sub>CC</sub>	0.40xV <sub>CC</sub>		
V <sub>DT3</sub>	DT mode select threshold 4	0.21xV <sub>CC</sub>	0.23xV <sub>CC</sub>	0.25xV <sub>CC</sub>		

**Package Details: SOIC16N**

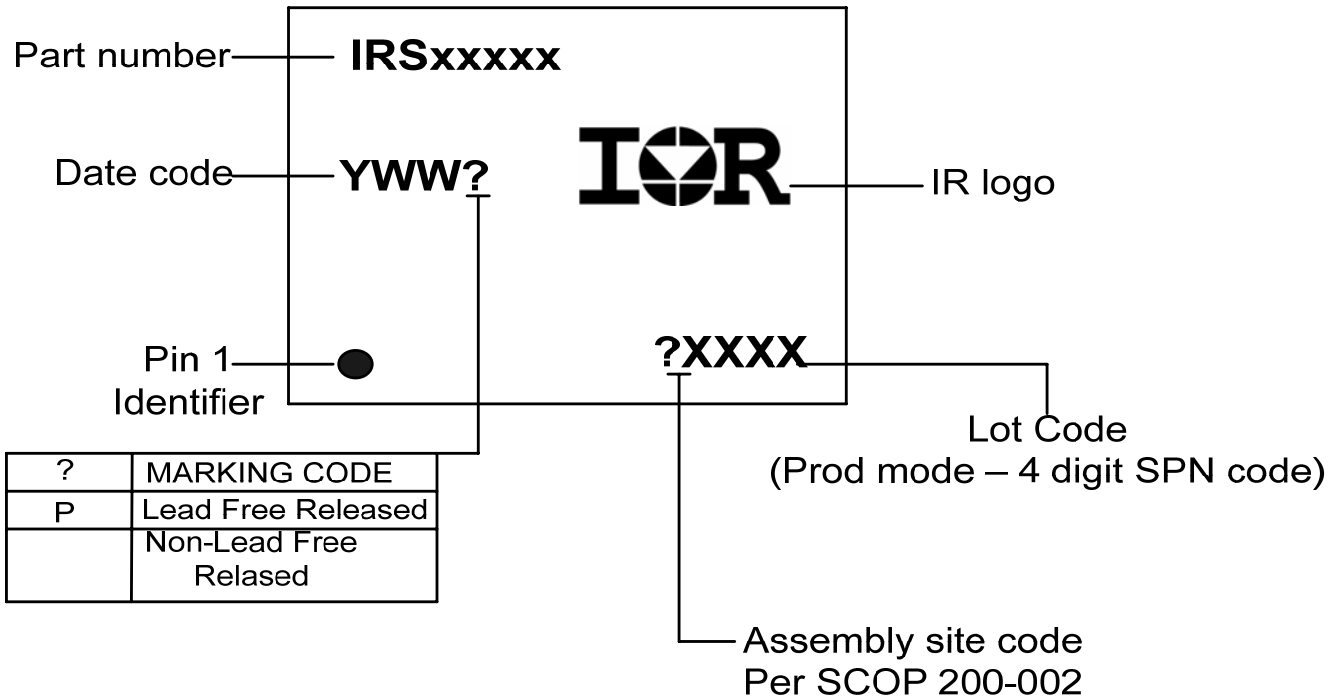


**NOTES:**

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AC.

- ⑤ DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
- ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

**Part Marking Information**





**Ordering Information**

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS2092	PDIP16	Tube/Bulk	25	IRS2092PBF
	SOIC16N	Tube/Bulk	45	IRS2092SPBF
		Tape and Reel	2500	IRS2092STRPBF